UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,404	10/08/2003	Luther A. Johnson	RPD 0045	7450

7590 03/16/2006

David G. Rasmussen
8 Hazel Rd
Hopkinton, MA 01748

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Office Action Summary	10/681,404	JOHNSON, LUTHER A.	
	Examiner	**Art Unit**	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) 1-9 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a)☐ All b)☐ Some * c)☐ None of:
  1.☐ Certified copies of the priority documents have been received.
  2.☐ Certified copies of the priority documents have been received in Application No. _____.
  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The meaning "counter is a count field in the lookup cache " is unclear. The counter specified in claim 1 is a program counter that is well known and claimed in claim 1 to contain an indicator of the address of the next instruction to be performed. This claimed contradicts the meaning of the program counter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yard (patent No. 5,892,934) in view of Gilson (patent No. 5,361,373).

6. Yard taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) First processor (12) for executing program instructions (e.g., see fig. 1);

b) Registers (54)(e.g., see figs. 2,3);

c) Function lookup unit (46) having a lookup cache with a tag field (92,94) and function identifier field (92,94 combined to indicate address indicative of function and tag sent instead on bus of address) (e.g., see fig. 7); (e.g., see col. 8, lines 32-52 ,col. 10, lines 39-67 and col. 12, line 40-col. 13, line 9) and comparing the address of the next instruction to be executed and a tag indicator[addresses for DSP routines stored a table are compared to the target address of the call instruction being executed where the target address of the call instruction being executed is the instruction of the next instruction to be executed] (e.g., see col. 11, lines 14-32). Also since Yard taught an embodiment of sends a shortened address or tag to the bus and the address in the table were stored as tags instead of the longer address (e.g., see col. 11, line 65-col. 12, line 6). One of ordinary skill would have been motivated to use the tags for the comparison at least to provide a quicker comparison. Yard taught that in response to a match between the target address of the call and the address stored in the table the function lookup unit, the lookup assumes control of the execution at the target address (e.g., See 11, lines 14-66) and when a match is not present a call to another processor is performed and the another processor takes control of execution of the instruction (e.g., see col. 11, lines 52-64).

7. Yard did not expressly detail (claim 1) that when the match was not present the first processor assumes control of the execution. Yard however taught the system may contain an indicator whether the DSP is enabled. If the DSP is not enabled then the microprocessor executes the original instruction routines stored at the target address of

the instruction (e.g., see col. 2, lines 12-25). Therefore one of ordinary skill would have been motivated to have the first processor to execute the operation when a match was not present. [the match would occur then the DSP that could perform the operation as the DSP was present and enabled, and when the DSP was not present and enabled the comparators would have would provide a no match result and the first processor would perform the operation at the next instruction address (target address)].

8. Yard did not expressly detail that the program counter was shared (claim 1). Yard taught that results were stored into register file (54) (e.g., see col. 7,lines 19-33). Yard also taught an embodiment where the DSP was included in the system (e.g,. see col. 5,lines 34-53 and when the DSP was executing an instruction the first processor was stalled. Therefore it would have been obvious to one of ordinary skill that the Yard system shared registers at least to store results in the available registers. Also since the system coupled the DSP to the same decoder as the other execution units one of ordinary skill would have been motivated to share the program counter between the DSP and the first processor.

9. Yard did not expressly detail (claim 1)the DSP comprised a reconfigurable combinatorial array. Gilson however taught (e.g., see fig. 1 and col. 6, lines 32-60) a reconfigurable combinatorial array having logic functions available that provide a mapping from the beginning state on entry to a block of code to an ending state from the block of code (e.g,. see col. 4 lines 36-65), the functions having identifiers in the function identifier field. As to the further limitation Gilson taught the DSP comprising FPGA receiving an function indicator that it uses to reconfigure the array to execute the

instruction (e.g., see col. 6, lines 29-66). Yard taught DSP receiving the function indicator identifiers from the lookup cache upon finding a match between the tag field and the program counter indicator, the function indicator identifiers causing the function to be executed in place of the block of instructions starting at the program counter indicator as discussed above.

10. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Yard and Gilson. Both references were directed to the problems of providing increased efficiently of processing by use of one or more DSPs . One of ordinary skill would have been motivated to add the Gilson teachings of the reconfigurable array as it would have allowed the combined system to processing instructions to be executed in software efficiently in hardware..

11. As per claim 2, Gilson taught a exception routine that provides logic synthesis (reconfigures the array of logic) for the instructions to be executed and providing a synthesized function to the reconfigurable combinational array and a corresponding function indicator (e.g., see col. 6, lines 1-67). Yard taught the program counter (target address) identified the block of instructions that the DSP performs and a response signal is sent to the DSP from the function lookup unit to initiate the operation of the DSP and a function identifier (tag) corresponded to the function identifier as discussed above.

12. As per claim 3,4 Gilson taught the preloading of the logic functions on the fly before executing the program instructions (the array is reconfigured before the instructions are executed) (e.g., see col. 6, lines 1-67)(e.g., see col. 7,lines 5-57).

13. As per claim 7,8,9 Yard taught that when the first processor processes an instruction that may be done by a DSP, the function is a call instruction that is sent to the function lookup processor and executed by the DSP and upon return the first processor processes from the instruction after the end of the block of instructions (e.g., see col. 3, lines 26-45). Since the program counter is a register that indicates the next instruction to be executed, when the call instruction was pointed to by the program counter the system would send the instructions to the DSP for processing. However in the event of a system error where the instruction was not to execute it one ordinary skill would have been motivated to send an indication of the program counter being overwritten to the function lookup unit search for matching address in the deactivate the processing by the DSP and the deactivation of the stored program address in the lookup cache. This would have been done at least to ensure that the system did not perform any unnecessary processing.

14. Claims 5,6, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yard and Gilson as applied to claim 1-4 above, and further in view of Greenbaum (patent No. 5,933,642).

15. Greenbaum taught (claims 5-6) nested loop of operations for which on the fly reconfiguration of FPGAs are required for operations of the various loops with directives to indicate the reconfiguration (e.g., see col. 6, lines 58-col. 7, line 57). Therefore since loops would have been performed multiple times and at the end of the loop another loop would have been performed (requiring reconfiguration of the FPGA) the one of ordinary skill would have been motivated to include a counter to count indicate the number of

times the block of instructions was executed and the branching to an exception routine indicated by the directive to reconfigure the FPGA. As understood (claim 6) a count field would have been necessarily providing an indication to the system how many times the loops would have to be executed. Storing the count field with the instructions in a cache was well known in the art at the time of the claimed invention.

Response to Arguments

Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hazelzet (patent No. 6,446,163) disclosed a memory card with signal processing element (e.g, see abstract and col. 3, lines 9-54)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER